FUNCTIONAL DESCRIPTION

When the CAT is operating as a SLAVE, control words can be loaded into Control Space Registers and Data Space Registers with standard FASTBUS protocol write operations. A yellow front-panel LED on the CAT indicates when it is addressed.

The CAT must be in data Acquisition Mode (AM) to provide trigger strobes. The Crate Master, usually a LeCroy Model 1821 Segment Manager Interface, can generate this as a broadcast. The CAT recognizes this condition and then uses the TR lines of the FASTBUS Segment to transmit its signals to the data acquisition modules. The TR lines are used to avoid interference with normal use of the Segment during data collection.

Timing control and distribution is the primary operation of the CAT. The three most important system strobes are the ADC Gate, the TDC Common Stop, and the ICA Common Stop. An additional signal, the Measurement Pause Interval (MPI) for use by the data acquisition modules is provided by the CAT. It is programmable from 0 to 63 μsec. The MPI time is usually used to permit a FAST CLEAR decision. After the MPI, the Slaves begin conversion. A Fast Clear pulse received at the CAT during the MPI restarts the TDC clock and applies a Fast Clear pulse to the ADC modules. At the end of the MPI, the CAT provides the trailing edge of the Common Stop pulse used by the DAMs to initiate their data conversion.

SPECIFICATIONS

INPUTS

ADC GATE: Defines the integrating time for ADCs. Distributed differentially to the LeCroy Models 1882/1885 via the TR1 and TR2 lines. Duration 50-2000 nsec. Begins the MPI.
TDC STOP: Begins the MPI. Minimum width 50 nsec. Distributed via the TR6 line.
ICA STOP*: Reserved for future use.
FAST CLEAR*: Distributes fast clear signal to ADC modules, restarts the TDC oscillators and terminates the MPI. Minimum width 50 nsec. Distributed via the TR0 line.
AFC STROBE*: Supplies a pulse to the personality cards to define the event time. Minimum width 50 nsec.
TDC/ICA TEST: Applies timing pulses to the TDCs. Used in conjunction with the Common Stop inputs. Minimum width 50 nsec. Distributed via the TR3 lines.

OUTPUTS

LEVEL OUT: Lemo connector output. Supplies 0 to +10 V DC level used to program the ADC test pulser. Output impedance 1 kΩ for front-panel output, 0.1 Ω on UR0 and UR1 lines.
MPI IN/MPI OUT: Bidirectional port used to synchronize the MPIs in all crates. Two identical Lemo connectors. Bidirectional current sink: output -28 mA at -1.4 V; input 50 Ω, -1.4 V to enable. When daisy chained, the duration of the MPI at all CATs in the daisy chain is equal to the duration of the longest MPI in the chain.
BUSY: NIM Lemo and ECL 2-pin header. False level indicates that the crate is in acquisition mode. True indicates a trigger has been received.
CAL TRIGGER: NIM Lemo and ECL 2-pin header. The pulse, typically 85 nsec, signifies that the crate is starting a test cycle.

CALIBRATION CONTROL

TDC (DSR0): Programs the time of the trailing edge of a time pulse, and the time of the stop pulse (20 bits/ 65.5 μsec maximum). Also enables and disables a second pulse approximately midway between pulse 1 and the Common Stop.
ADC (DSR3): A 12-bit amplitude word. Sets the amount of charge injected into each ADC channel when the test feature is enabled.

GENERAL

Power Requirements: 50 mA at +15 V; 1.0 A at +5 V; 4.0 A at -2 V; 6.5 A at -5.2 V; 100 mA at -15 V.
Packaging: Single-width FASTBUS module in conformance with FASTBUS specification IEEE-960.

FASTBUS CONTROL

Addressing Modes: Geographical, Secondary, Broadcast. Broadcast Address Implemented:

Code	*Significance*	*Comments*
$(0D)_h$**	All device scan	The 1810 asserts its "T" pin on following read cycles.
$(8D)_h$	FAST CLEAR	Generates 50 nsec pulse on TR0. OR'd with front-panel FAST CLEAR.

Slave Status Response to Data Cycles:

SS	*Significance*
0	Valid action
6	Error, data rejected
7	Invalid secondary address

CONTROL FUNCTIONS IMPLEMENTED

Module Identification Code: (Read only CSR0) $(1039)_h$
Test Pulse: Disable, enable single & double pulse.

* Two inputs, one bridged high impedance Lemo pair accepting NIM inputs, and one 110 Ω impedance (removable SIPs) 2-pin header accepting differential ECL inputs.
** An h subscript denotes a hexadecimal number, i.e., base 16.